Efficient Logic Design Using Spin Transfer Torque Memory Technology & Lookup Tables

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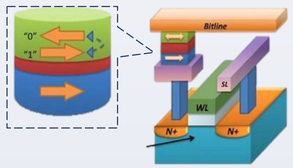
Research Goals

- Hybrid design of logic circuits using custom CMOS and STT-LUTs
- Optimal hybridizations that utilizes efficiency of custom CMOS and programmability of Lookup Tables
- Experiment this optimization on adder test circuit

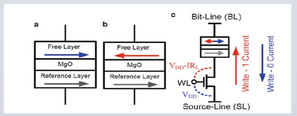
Spin Transfer Torque Random Access Memory (STTRAM)

- STT technology offers non-volatile information storage using Magnetic Tunnel Junctions (MTJ)
- Offers more flexibility compared to current information storage technology such as DRAM, SRAM
- Reconfigurable memory technology

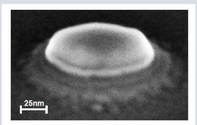


Magnetic Tunnel Junction

- Composition
  - 2 ferromagnetic layers Includes:
    - Free layer - magnetic field orientation can be changed
    - Fixed layer - magnetic field orientation cannot be changed
  - Oxide barrier
- Used to store information
  - Information is sensed as resistances
  - Resistance is sensed by applying a current to MTJs layers
  - Low resistance is logic state 0
  - High resistance is logic state 1

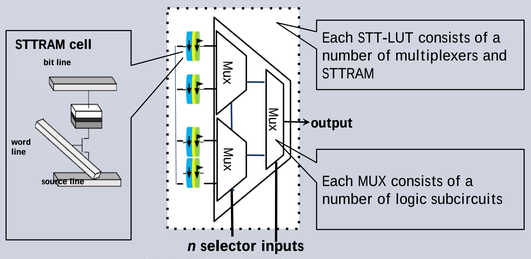


STT-RAM basics: (a) Parallel (Low Resistance). (b) Anti-parallel (high Resistance). (c) 1T1MTJ cell structure [Weisheng Zhao, 2015]



Microscopic view of MTJ [T. Kawahara, Microelectronics Reliability Jr.]

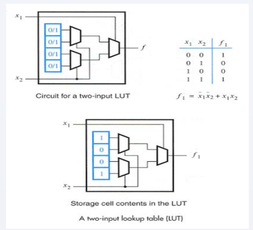
STT Based Look Up Table (STT-LUT)



[Hamid Mahmoodi, 2016]

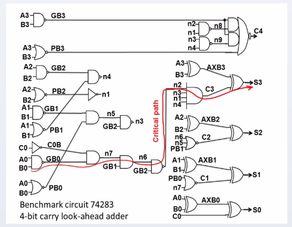
Logic Implementation using STT-LUT

- Contents of STT-LUTs can be programmed to implement any arbitrary logic function
- STT-LUTs improve security and are non-volatile
- Require more time, power, and transistors to operate



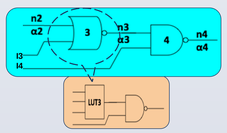
Case Study: 4-bit Adder

- Gate-level schematic of 4-bit adder showing the critical path, which is the pathway with the most delay and passes the most number of gates
- LUT replacement of all the gates on the critical path causes delay overhead
- LUT replacement of some non-critical gates results in delay overhead and change of the critical path



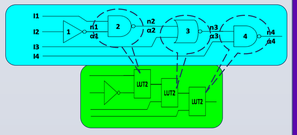
Individual Gate Mapping

- Each logic gate can be replaced by Lookup Table programmed with the corresponding truth table of the logic gate
- Simulate and extract data from each mapped gate



Multiple Gate Mapping

- Map multiple gate simultaneously and extract data
- Three optimization algorithms
  - Independent Selection
  - Dependent Selection
  - Parametric-Aware Dependent Selection



Independent Selection

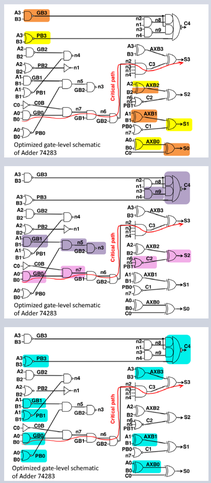
- Randomly select gates in which their paths do not intersect

Dependent Selection

- Gates that are along the same path or subsequent to each other are mapped

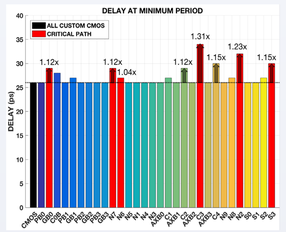
Parametric-Aware Dependent Selection

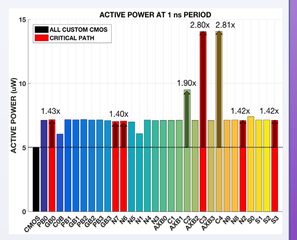
- Gates that do not greatly impact delay are mapped



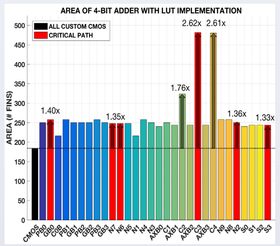
Individual Gate Mapping Results

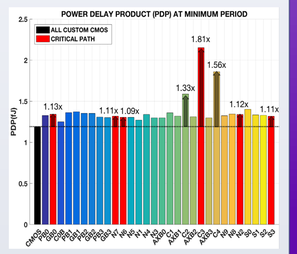
All the 30 gates in the 4-bit adder were individually mapped to measure the time delay, active power consumption, area and power delay product. Data is then compared to that of all Custom CMOS.





- LUT replacement of a gate may result in delay overhead
- LUT replacement of any gate results in power overhead

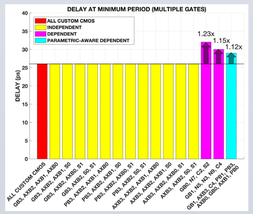


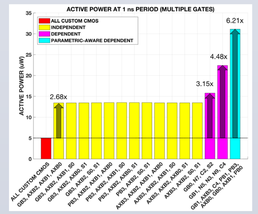


- LUT replacement of any gate results in area increase
- PDP is the most accurate way to compared all the mapped gates

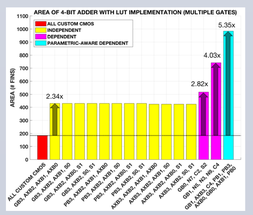
Multiple Gate Mapping Results

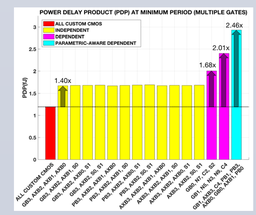
Multiple gates were selected using the algorithms and the individual mapping results. Most gates that produced delay overhead were not selected. Selected gates with delay overhead were chosen to protect vulnerability.





- Independent selection produced no delay overhead
- Parametric-aware dependent selection required the most power

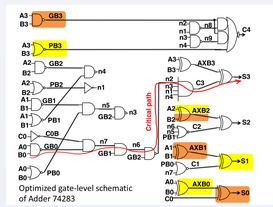




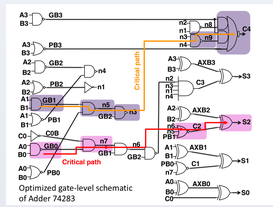
- Parametric-aware dependent selection occupies the most area
- Parametric-aware dependent selection rated highest in PDP

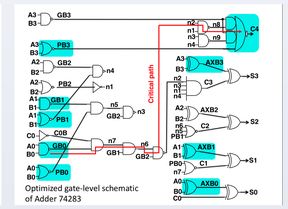
Change in Critical Output

The critical output is the indication of where the critical path ends. When mapping the gates, we also focused on the whether or not the critical output changes. This change in the critical output meant that the critical path had changed as well; this tells us which specific mappings cause significant delay.



- Critical path does not change when mapping independent selections
- Critical path changes when mapping dependent and parametric-aware dependent selections





Conclusion

Independent selection causes no delay overhead and uses the least power to operate but is the easiest to reverse-engineer. Dependent selection is more difficult to reverse-engineer but shows the longest delay overhead. Parametric-aware dependent selection is more difficult to reverse-engineer than independent and has less delay than dependent but requires more power. Depending on the designer's preference, a different algorithm would be selected. If performance is prioritized over all else, the independent selection algorithm would be used. If the main purpose of the hybrid design is to improve security while minimizing power, the dependent selection should be applied. If power consumption is not an issue, parametric-aware dependent selection would be used since it offers more reconfigurabilty with some delay.

References

[1] Almasi, D., *Enhancing Hardware Security Using Spin Transfer Torque Logic*, in *Engineering of Embedded Electrical and Computer Systems*. 2015, San Francisco State University: San Francisco.
[2] Mano, M. Morris and Kime. Charles R. *Logic and Computer Design Fundamentals*. New Jersey: Pearson Education, 2008. Book.
[3] Winograd, T., et al., Preventing design reverse engineering with reconfigurable spin transfer torque LUT gates, in 17th International Symposium on Quality Electronic Design. 2016, IEEE: Santa Clara, CA. p. 242-247.
[4] C. Augustine et. al., "Spin-Transfer Torque MRAMs for Low Power Memories: Perspective and Prospective," IEEE Sensors Journal, vol. 12, no. 4, pp. 756 – 766, 2012.
[5] Almasi D., Mahmoodi, H. Homayoun, H. Salmani, H. "Device and Circuit Optimizations for Spin Transfer Torque Reconfigurable Logic"

Acknowledgments

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